REMARKS

Reconsideration and allowance are respectfully requested. Claims 2 and 7 have been amended. Claims 1-10 are pending in the application.

Claims 1-10 stand rejected under 35 USC §103(a) as being obvious over U.S. Patent No. 6,988,161B2 to McConnell et al. This rejection is respectfully traversed.

The Examiner states that McConnell et al., at column 10, lines 19-23, "explicitly recites physical links, which are different from link widths". Applicant is not sure what the Examiner is trying to convey by this statement. Clarification is requested.

Claim 1 recites setting a multiplexer circuit, configured for selectively switching frame data of a prescribed maximum link width to a selected one of a plurality of available link widths, to the selected active link width, receiving the frame data from an output buffer according to the prescribed maximum link width and outputting the frame data from the multiplexer circuit to a transmit bus according to the selected active link width. Thus, the multiplexer circuit is configured for switching frame data of a prescribed maximum link width **to** the selected active link width. Claim 6 has similar features.

Applicant submits that the port in Fig. 6 of McConnell et al. does not combine/multiplex virtual lanes, it is the InfiniBand™ protocol that does. As described at page 5, lines 13-16 of the specification, multiplexing virtual lanes on a single port is well known in the InfiniBand™ architecture. This is not what is being claimed. For example, claim 1 recites setting a multiplexer circuit to the selected link width. Even if McConnell et al. can be considered to have a multiplexing circuit, there is no disclosure or suggestion of a multiplexer circuit receiving the frame data from an output buffer according to the prescribed maximum link width (see the 108 bit input bus 96 of FIG. 3 of the specification) and setting the multiplexer circuit to the selected link width in McConnell et al. Each of the independent claims specifies the multiplexer circuit configured for "selectively ***switching*** frame data of a prescribed maximum link width". As described in

the specification, the "switching" in the multiplexer of Figure 3 includes not only transfer of data, but transfer of the data according to the appropriate width, and the appropriate sequence for transmissions using link widths smaller than the prescribed maximum link width. This is simply not disclosed or suggested in McConnell et al. There is no concept of maximum link width in the virtual lane disclosure of McConnell et al.

For these reasons, the §103 rejection should be withdrawn because the rejection fails to establish that the applied reference teaches the claimed features. It is well settled that each and every claim limitation must be taught or suggested. As specified in MPEP §2143.03, entitled "**All Claim Limitations Must Be Taught or Suggested**": "To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). 'All words in a claim must be considered in judging the patentability of that claim against the prior art.' *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970)." MPEP §2143.03 at 2100-131 (Rev. 5, Aug. 2006).

Accordingly, the rejection of claims 1 and 6, and the claims that depend therefrom, should be withdrawn

With regard to claims 2 and 7, these claims have been amended to recite a first multiplexer for outputting the frame data onto a first output according to a first of the available link widths, and a second multiplexer circuit, distinct from the first multiplexer, configured for switching the frame data onto a second output according to a second of the available link widths. There is simply no teaching in McConnell et al. of a first multiplexer and a distinct, second multiplexer circuit as claimed for outputting frame data according to different available link widths. The Examiner mentions "multiplexing means (circuit)" of Fig. 6 of McConnell et al. but cannot identify first and second multiplexer circuits in McConnell et al. since no such circuits are shown or described. Therefore, the rejection should be withdrawn.

In view of the above, it is believed this application is in condition for allowance, and such a Notice is respectfully solicited.

To the extent necessary, Applicant petitions for an extension of time under 37 C.F.R. 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including any missing or insufficient fees under 37 C.F.R. 1.17(a), to Deposit Account No. 50-0687, under Order No. 95-520, and please credit any excess fees to such deposit account.

Respectfully submitted,

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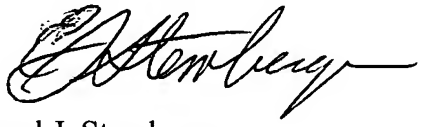

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